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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,089	UHLER, G. MICHAEL	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-32 and 37-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-32 and 37-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20050120*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention.

2. Claims 1-7, 9 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

3. It is unclear how, in Claim 1, an interrupt register, which is a physical object, is connected to a vector table, which is a data structure.

4. In Claim 22, it is unclear if the priorities of the first interrupts established by the interrupt controller are the same as the architecturally fixed interrupt priorities of Claim 10. It is further unclear how an architecturally fixed interrupt priority can be established by an interrupt controller, as this requires some means for the interrupt priorities to be programmed by the interrupt controller, and thus are not architecturally fixed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 10 are rejected under 35 U.S.C. 102(b) as being anticipated by the Motorola MCF5206 Integrated Microprocessor, as described in Freescale Semiconductor, Inc. Product Brief "MCF5206 Integrated Microprocessor" ("MCF5206") and Freescale Semiconductor, Inc. "Addendum to MCF5206 User Manual" ("MCF5206 Addendum").

7. In reference to Claim 10, MCF5206 discloses a microprocessor for handling interrupts, the microprocessor receiving first interrupts from an interrupt controller, the first interrupts having architecturally fixed interrupt priorities (See 'Interrupt Controller' on Page 5), the microprocessor comprising: a core for executing instructions (See Page 1 Paragraph 3), said core generating second interrupts (See 'Interrupt Controller' on Page 5). Because the interrupt priorities are programmable, MCF5206 will inherently include priority storage logic for storing the programmable priorities of the second interrupts (See 'Interrupt Controller' on Page 5). MCF5206 will inherently have a priority encoder coupled to the core for prioritizing the first and second interrupts utilizing the fixed

priorities for the first interrupts and the programmable priorities for the second interrupts (See Page 2 'System Interface' – 'Programmable Interrupt Controller').

8. In reference to Claim 11, MCF5206 discloses the limitations as applied to Claim 10 above. MCF5206 further teaches that the interrupt controller receives a plurality of third interrupts from sources thereof, prioritizes said third interrupts, and provides the prioritized third interrupts to the microprocessor as the first interrupts (See 'Interrupt Controller' on Page 5).

9. In reference to Claim 12, MCF5206 discloses the limitations as applied to Claim 11 above. MCF5206 further discloses that the first interrupts are presented to the processor on first interrupt signal lines attached to the microprocessor (See Figure on Page 6).

10. In reference to Claim 13, MCF5206 discloses the limitations as applied to Claim 10 above. MCF5206 Addendum discloses that the instructions executed by the core of the MCF5206 comprise: JSR, BSR, and RTS instructions, which are both instructions for handling the first interrupts and instructions for handling the second interrupts (See Pages 3-5). MCF5206 further discloses third instructions for storing said programmable priorities into said priority storage means (See 'Interrupt Controller' on Page 5).

11. In reference to Claim 14, MCF5206 discloses the limitations as applied to Claim 10 above. MCF5206 further discloses that the plurality of first interrupts comprise timer interrupts, which are hardware interrupts (See 'Timer Module' on Page 4). MCF5206 Addendum discloses that the MCF5206 also includes a TRAP instruction, which is a software interrupt (See Page 5).

12. In reference to Claim 16, MCF5206 discloses the limitations as applied to Claim 10 above. MCF5206 further discloses that that there are a plurality of internal interrupts that can each be programmed to a different priority (See 'Interrupt Controller' on Page 5), and thus the priority storage logic must inherently include a plurality of interrupt fields each corresponding to one of the second interrupts.

13. In reference to Claim 17, MCF5206 discloses the limitations as applied to Claim 16 above. MCF5206 further discloses that each internal interrupt signal can be programmed to one of 7 interrupt levels each having 4 priority levels (See 'Interrupt Controller' on Page 5), thus providing 28 distinct interrupt priorities which require a minimum 5-bit field (which allows a maximum of 32 distinct values) to store. A 4-bit field is a subset of a 5-bit field, and thus a 4-bit field providing 16 distinct interrupt priorities is inherently a part of MCF5206.

14. In reference to Claim 20, MCF5206 discloses the limitations as applied to Claim 10 above. MCF5206 further discloses that each external interrupt signal can be

programmed to one of 3 interrupt levels each having 4 priority levels (See 'Interrupt Controller' on Page 5), thus providing 12 distinct interrupt priorities. Eight distinct interrupt priorities is a subset of a 12 distinct interrupt priorities, and thus 8 distinct interrupt priorities for the first interrupts is inherently a part of MCF5206.

15. In reference to Claim 21, MCF5206 discloses the limitations as applied to Claim 20 above. MCF5206 further discloses that each internal interrupt signal can be programmed to one of 7 interrupt levels each having 4 priority levels (See 'Interrupt Controller' on Page 5), thus providing 28 distinct interrupt priorities . The 28 internal interrupt levels overlap with the 12 external interrupt levels (See 'Interrupt Controller' on Page 5).

16. In reference to Claim 22, MCF5206 discloses the limitations as applied to Claim 10 above. MCF5206 further discloses that that the priority encoder, when prioritizing the first and second interrupts, also uses priorities for the first interrupts established by the interrupt controller (See 'Interrupt Controller' on Page 5).

17. In reference to Claim 23, MCF5206 discloses the limitations as applied to Claim 10 above. The priority encoder of MCF5206 will inherently produce an indication of which of the first and second plurality of interrupts has the highest priority.

18. In reference to Claim 24, MCF5206 discloses the limitations as applied to Claim 23 above. MCF5206 further discloses a vector generator for producing an interrupt vector corresponding to the interrupt having the highest priority (See Page 2 'System Interface' – 'Programmable Interrupt Controller').

19. In reference to Claim 27, MCF5206 discloses a method for prioritizing on-core and off-core interrupts in a processing system, comprising: receiving the off-core interrupts, the off-core interrupts having architecturally fixed interrupt priorities (See 'Interrupt Controller' on Page 5); receiving the on-core interrupts, the on-core interrupts having programmable priority levels which are intermediate to the architecturally fixed interrupt priorities for the off-core interrupts (See 'Interrupt Controller' on Page 5). MCF5206 will inherently prioritize the on-core and off-core interrupts according to their priority levels produce an indication of which of the first and second plurality of interrupts has the highest priority.

20. In reference to Claim 29, MCF5206 discloses the limitations as applied to Claim 27 above. MCF5206 further discloses that the off-core interrupts are initially prioritized by an interrupt controller (See 'Interrupt Controller' on Page 5).

21. In reference to Claim 30, MCF5206 discloses the limitations as applied to Claim 27 above. MCF5206 will inherently select the received on-core or off-core interrupt with

the highest priority level by examining the priority levels of each of the received on-core and off-core interrupts (See 'Interrupt Controller' on Page 5).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 1 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Motorola MCF5206 Integrated Microprocessor, as described in MCF5206 and MCF5206 Addendum, in view of US Patent Number 6,499,078 to Beckert et al. ("Beckert").

24. In reference to Claim 1, MCF5206 teaches a plurality of first interrupts, generated by a core, said plurality of first interrupts having programmable priorities (See 'Interrupt Controller' on Page 5); a plurality of second interrupts that are generated external to the core, said second interrupts having architecturally fixed priorities (See 'Interrupt Controller' on Page 5). MCF5206 will inherently have a priority encoder coupled to the first and second interrupts and a vector generator for prioritizing the interrupts utilizing programmable priorities for the first interrupts and fixed priorities for the second

interrupts (See Page 2 'System Interface' – 'Programmable Interrupt Controller'). MCF5206 further teaches storing a programmable interrupt value for the internal interrupts (See "'Interrupt Controller' on Page 5) and a vector generator (See Page 2 'System Interface' – 'Programmable Interrupt Controller') but is silent as to the structure. Beckert teaches an interrupt controller having interrupts with programmable priorities, having a status register (See Figure 2 Number 40), said status register comprising a vector table (See Figure 2 Number 50), and an interrupt register, said interrupt register coupled to said vector table, said interrupt register having a plurality of configurable priority registers for storing said programmable priorities (See Figure 2 Number 48 and Column 3 Line 61 – Column 4 Line 42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of MCF5206 with priority value storage means and vector table storage means of Beckert, resulting in the invention of Claim 1, because MCF5206 is silent as to the structure of how it stores the interrupt priority values and vector table, and one would naturally look to interrupt systems having programmable priorities when constructing the device, and because the priority registers and address registers provide an easy means for changing the priority levels and servicing information for any given interrupt source (See Column 2 Lines 11-22 of Beckert).

25. In reference to Claim 2, MCF5206 and Beckert teach the limitations as applied to Claim 1 above. MCF5206 further teaches that the plurality of first interrupts comprise

timer interrupts, which are hardware interrupts (See 'Timer Module' on Page 4). MCF5206 Addendum teaches that the MCF5206 also includes a TRAP instruction, which is a software interrupt (See Page 5).

26. In reference to Claim 4, MCF5206 and Beckert teach the limitations as applied to Claim 1 above. MCF5206 further teaches that the core executes instructions (See Page 1 Paragraph 3).

27. In reference to Claim 5, MCF5206 and Beckert teach the limitations as applied to Claim 1 above. MCF5206 further teaches providing the plurality of second interrupts to the priority controller with predefined interrupt priorities (See 'Interrupt Controller' on Page 5).

28. In reference to Claim 6, MCF5206 and Beckert teach the limitations as applied to Claim 1 above. The priority encoder of MCF5206 will inherently produce an indication of which of the first and second plurality of interrupts has the highest priority.

29. In reference to Claim 7, MCF5206 and Beckert teach the limitations as applied to Claim 6 above. MCF5206 further teaches a vector generator for producing an interrupt vector corresponding to the interrupt having the highest priority (See Page 2 'System Interface' – 'Programmable Interrupt Controller').

30. In reference to Claim 9, MCF5206 and Beckert teach the limitations as applied to Claim 1 above. Beckert further that the configurable priority registers are writable by the processing system (See Column 3 Lines 1-9).

31. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over MCF5206, MCF5206 Addendum, and Beckert as applied to Claim 2 above, and further in view of US Patent Number 5,768,500 to Agrawal et al. ("Agrawal").

32. In reference to Claim 3, MCF5206, MCF5206 Addendum, and Beckert teach the limitations as applied to Claim 2 above. MCF5206 further teaches that interrupts can be generated by hardware timers (See 'Timer Module' on Page 2). MCF5206, MCF5206 Addendum, and Beckert do not teach that said hardware interrupts comprise a performance counter interrupt. Agrawal teaches the use of a performance counter interrupt (See Column 8 Lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of MCF5206, MCF5206 Addendum, and Beckert with the performance counter and interrupt of Agrawal, resulting in the invention of Claim 3, in order to allow development of a cache miss profile by allowing the system to sample the state of the processor at a predetermined number of cache misses as well as to provide assistance in isolating performance bottlenecks and guiding optimization architectures, operating systems, compilers, and applications (See Column 1 Line 50-Column 2 Line 6 of Agrawal).

33. Claims 15 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over MCF5206, MCF5206 Addendum as applied to Claims 10 and 27 above, and further in view of Agrawal.

34. In reference to Claim 15, MCF5206 and MCF5206 teach the limitations as applied to Claim 10 above. Larsen further teaches that interrupts can be generated by internal hardware timers (See Column 5 Lines 60-63). MCF5206 further teaches that interrupts can be generated by hardware timers (See 'Timer Module' on Page 2). MCF5206, and MCF5206 Addendum do not teach that said hardware interrupts comprise a performance counter interrupt. Agrawal teaches the use of a performance counter interrupt (See Column 8 Lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of MCF5206 and MCF5206 Addendum with the performance counter and interrupt of Agrawal, resulting in the invention of Claim 15, in order to allow development of a cache miss profile by allowing the system to sample the state of the processor at a predetermined number of cache misses as well as to provide assistance in isolating performance bottlenecks and guiding optimization architectures, operating systems, compilers, and applications (See Column 1 Line 50-Column 2 Line 6 of Agrawal).

35. Claim 28 recites limitations that are substantially equivalent to those of Claim 15 above, and is rejected under similar reasoning.

36. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over MCF5206 as applied to Claim 10 above, and further in view of US Patent Number 5,148,544 to Cutler et al. ("Cutler").

37. In reference to Claim 18, MCF5206 teaches the limitations as applied to Claim 10 above. MCF5206 does not teach that said priority storage means is located within a privileged resource within the microprocessor. Cutler teaches that a register for storing information related to an interrupt condition is accessible only during a privileged mode (See Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of MCF5206 with the privileged mode register access of Cutler, resulting in the invention of Claim 18, in order to prevent a compromise of the security of other users or programs (See Column 7 Lines 37-40 of Cutler).

38. In reference to Claim 19, MCF5206 and Cutler teach the limitations as applied to Claim 18 above. Cutler further teaches that the privileged mode of operation during which the interrupt registers can be accessed is a kernel mode of operation (See Abstract).

39. Claims 25, 26, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over MCF5206 as applied to Claims 24 and 30 above, and further in view of US Patent Number 5,940,587 to Zimmer ("Zimmer").

40. In reference to Claim 25, MCF5206 teaches the limitations as applied to Claim 24 above. MCF5206 does not teach programmable offset storage means, coupled to said vector generator, for providing a programmed offset to said vector generator to allow said vector generator to produce said interrupt vector. Zimmer teaches a programmable offset storage means for providing a programmed offset to said vector generator to allow said vector generator to produce said interrupt vector (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of MCF5206 with the programmable offset storage means of Zimmer, resulting in the invention of Claim 25, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

41. In reference to Claim 26, MCF5206 and Zimmer teach the limitations as applied to Claim 25 above. Zimmer further teaches that the interrupt vector table containing the

offset values is created by a system executive, which is equivalent to kernel mode instructions (See Column 3 Lines 30-41).

42. In reference to Claim 31, MCF5206 teaches the limitations as applied to Claim 30 above. MCF5206 does not teach examining a programmable offset and calculating an interrupt vector for the one of the interrupts with the highest priority level utilizing said programmable offset. Zimmer teaches a programmable offset storage means for providing a programmed offset to said vector generator to allow said vector generator to calculate said interrupt vector (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of MCF5206 with the programmable offset storage means of Zimmer, resulting in the invention of Claim 31, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

43. In reference to Claim 32, MCF5206 and Zimmer teach the limitations as applied to Claim 31 above. MCF5206 inherently jumps to the interrupt vector in order to access the proper interrupt handler.

Claim Rejections - 35 USC § 101

44. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

45. Claims 37-39 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 37-39 are directed to a computer data signal embodied in a computer readable transmission medium. A computer data signal is neither a process, machine, manufacture, nor composition of matter. Further, a computer data signal embodied in a computer readable transmission medium can be interpreted to be an electromagnetic wave propagating through free space, which is not tangible and thus is non-statutory.

Response to Arguments

46. Applicant's arguments with respect to claims 1-7, 9-32, and 37-39 have been considered but are moot in view of the new ground(s) of rejection.

47. In response to Applicant's statements regarding the status register (See Page 10 Paragraph 3), the Examiner will interpret the status register to include the vector table and the interrupt register.

48. Applicant has argued that Claims 37-39 meet the statutory requirements of 35 USC §101. Claims 37-39 are directed to a computer data signal embodied in a computer readable transmission medium. A computer data signal is neither a process, machine, manufacture, nor composition of matter, and thus does not meet the statutory requirements. Further, a computer data signal embodied in a computer readable transmission medium can be interpreted to be an electromagnetic wave propagating through free space, which is not tangible and thus is non-statutory. The Examiner further notes that both wireless Ethernet and Bluetooth are not tangible transmission media, as they are both specifications for communicating between devices using electromagnetic waves.

Conclusion

49. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 4,218,739 to Negi et al.; US Patent Number 4,626,985 to Briggs; US Patent Number 5,481,725 to Jayakumar et al.; US Patent Number 5,594,905 to Mital; US Patent Number 6,148,321 to Hammond; US Patent Application Publication Number 2003/0023799 to Yoo et al.; and US Patent Application Publication Number 2003/0088723 to Mackey et al.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-

3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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